PAPER TITLE

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Abstract: This paper presents a modified design of Area-Efficient Low power Carry Select Adder (CSLA) Circuit. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position, the speed of addition is limited by the time required to transmit a carry through the adder. Carry select adder processors and systems. Has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries.

Index terms: Area-efficient, Low power, CSLA, Binary to excess one converter, Multiplexer.